WE CLAIM AS OUR INVENTION:

1. A mail-processing device comprising:

at least one printhead;

a pixel memory containing binary pixel data, representing information to be printed by said at least one printhead, stored as a plurality of data strings consisting of successive data words with a predefined number of successive data words forming a data string;

a print data controller having access to said pixel memory and connected to said at least one printhead for controlling printing of said information by said at least one printhead, said print data controller comprising a DMA controller and an address generator and, for each printhead, a print data editing unit, the print data editing unit containing two buffer memories; and

said DMA controller transferring said binary pixel data word-by-word from said pixel memory into said two buffer memories with successive words in one of said data strings being alternatingly entered into one of said two buffer memories, for intermediate storage therein, said print data editing unit edits the data words stored in the other of said two buffer memories at respective addresses designated by said address generator, with said printhead printing the information represented by the data word stored in said other of said buffer memories.

2. A mail-processing device as claimed in claim 1 wherein said DMA controller generates address write signals and selection signals relating to said intermediate storage of said data words in said two buffer memories, said address generator generates and supplies said address signals and control signals to said

pixel data editing unit, and with said pixel data editing unit using said data words respectively stored in said buffer memories for editing in said pixel data editing unit in selected groups and in a selected sequence dependent on said address signals and said control signals.

3. A mail-processing device as claimed in claim 1 wherein said DMA controller generates address write signals and uses said address write signals to write said data words of said data string from said pixel memory respectively into said two buffer memories, and includes a cycle counter for counting said predefined number of data words.

4. A mail-processing device as claimed in claim 1 wherein said printer controller comprises a switchover signal generator, which generates a switchover signal supplied to said pixel data editing unit, for controlling the editing of the respective data words, by said pixel data editing unit, and using said at least one printhead for printing said information, and wherein said switchover signal generator also supplies said switchover signal to said DMA controller, and wherein said DMA controller generates respective selection signals, dependent on said switchover signal, for causing transfer of another data word from said pixel memory into said print data editing unit.

5. A mail-processing device as claimed in claim 1 comprising first and second printheads, and wherein said print data controller comprises a first print data editing unit having two buffer memories and a second print data editing unit having two buffer memories, and wherein said DMA controller includes a cycle counter, and wherein said print data controller generates a switchover signal supplied to said DMA controller, and wherein said DMA controller includes a first comparator and a second comparator, and wherein said DMA controller generates a DMA start signal

which causes said cycle counter to begin counting a predetermined number of data words in said data string from said pixel memory, and wherein said first comparator, dependent on said switchover signal, causes said DMA controller to supply a respective selection signal to said first pixel data editing unit until said predetermined number of data words is reached, and for causing said DMA controller to supply a respective selection signal to said second pixel data editing unit after said predetermined number of data words is reached, and wherein said second comparator generates a DMA busy signal having a zero value after a second predetermined number of data words is counted by said cycle counter, to end counting by said cycle counter.

6. A mail-processing device as claimed in claim 5 wherein each of said first and second pixel data editing units comprises a shift register operable in combination with the two buffer memories in that pixel editing unit, for parallel-to-serial conversion of said pixel data and wherein said address generator generates a load signal supplied to the shift register in each of said first and second print data editing units to cause loading of serial data from the respective print registers to the respective first and second printheads.

7. A mail-processing device as claimed in claim 6 wherein said address generator generates an address read signal having a plurality of bits, including more significant bits which designate an address in the first and second buffer memories, and less significant bits which allow addressing within a data word.

8. A mail-processing device as claimed in claim 1 comprising a transfer arrangement for conveying items past said at least one printhead on which said information is to be printed by said at least one printhead, said transfer arrangement including an encoder which generates encoder signals indicating a position of an

item relative to said at least one printhead, and wherein said print data controller includes a printer controller having a data string counter, said data string counter being incremented after each data string is printed, and wherein said printer controller supplies a signal to said at least one printhead ending printing of said information when said data string counter reaches a predetermined count.

9. A mail-processing device as claimed in claim 1 wherein said print data controller comprises a printer controlled connected to said DMA controller, said printer controller generating a DMA start signal and supplying said DMA start signal to said DMA controller, and wherein said DMA controller comprises a cycle counter for counting said data words, starting upon receipt of said DMA start signal, and wherein said DMA controller subsequently generates a DMA busy signal having a value zero and supplies said DMA busy signal to said printer controller.

10. A mail-processing device as claimed in claim 1 wherein each of said buffer memories is a dual port RAM.

11. A mail-processing device as claimed in claim 10 wherein said print data controller comprises a first multiplexer having inputs connected to a first of said dual port RAMs, a second multiplexer having inputs connected to a second of said dual port RAMs, a third multiplexer having inputs connected to respective outputs of said first and second multiplexers, a demultiplexer having an input connected to an output of said third multiplexer and a collecting register having inputs connected to outputs of said demultiplexer, said first multiplexer selecting a single bit of said pixel data from said first of said dual port RAMs when less-significant bits of an address read signal, generated by said address generator, is supplied thereto, and wherein said second multiplexer selects a single bit of pixel data from said second of said dual port RAMs, and wherein said second multiplexer, dependent on a switchover signal

generated by said print data controller, transfers the respective bits from said first and second multiplexers to said demultiplexer, and wherein said demultiplexer transfers successive single bits into said collecting register at respective addresses determined by an address signal supplied to said demultiplexer.

12. A mail-processing device as claimed in claim 11 further comprising a shift register connected to said collecting register, for transferring said bits from said collecting register to said at least one printhead.

13. A mail-processing device as claimed in claim 1 wherein said print data controller is an application-specific integrated circuit.

14. A mail-processing device as claimed in claim 1 wherein said print data controller comprises a programmable logic chip.